IN THE CLAIMS:

We claim:

1. A microelectronic system comprising at least one package having first and second circuit systems, each of said first and second circuit systems having means for wirelessly communicating with each other through at least one substrate.

2. The microelectronic system according to Claim 1, wherein the first and second circuit systems have identical operational formats.

3. The microelectronic system according to Claim 1, wherein the first and second circuit systems have different operational formats.

4. The microelectronic system according to Claim 1, wherein the at least one substrate is transparent.

5. The microelectronic system according to Claim 1, wherein the first and second circuit systems are one of a communication device and a chip.

6. The microelectronic system according to Claim 1, wherein the first and second circuit systems are fabricated on the at least one substrate.

7. The microelectronic system according to Claim 1, wherein the first and second circuit systems are bonded to the at least one substrate.

8. The microelectronic system according to Claim 1, wherein the package is fabricated by an alignment process which includes the steps of:

providing a photoresist on a top and bottom side of said at least one substrate;

irradiating said photoresist from at least one side of said at least one substrate to form an alignment pattern on said top and bottom side of said at least one substrate;

etching said alignment pattern to form global alignment marks on said top and bottom

sides of said at least one substrate; and

providing at least one communication device on one side of said at least one substrate using at least one global alignment mark as a reference point.

9. The microelectronic system according to Claim 1, wherein the first and second circuit systems include first and second interconnection structures for interconnecting the components of the first and second circuit systems, respectively.

10. The microelectronic system according to Claim 9, wherein the first and second interconnection structures are connected to a substrate.

11. The microelectronic system according to Claim 1, wherein the at least one substrate includes alignment marks for aligning the at least one substrate with alignment marks of another substrate.

12. The microelectronic system according to Claim 1, wherein the package is fabricated by an alignment process which includes the steps of:

providing an opaque layer on one side of said at least one substrate;

providing a photoresist on said opaque layer on one side of said at least one substrate;

irradiating said photoresist from at least the one side of said at least one substrate to form a first alignment pattern on said one side of said at least one substrate;

etching said first alignment pattern to form a first set of global alignment marks on said one side of said at least one substrate;

providing a photoresist on the other side of said at least one substrate;

irradiating said first alignment pattern from at least the one side of said at least one substrate to form a second alignment pattern on the other side of said at least one substrate;

etching said second alignment pattern to form a second set of global alignment marks on the other side of said at least one substrate, wherein the first and second sets of global alignment marks align with respect to each other; and

providing at least one communication device on said one side of said at least one substrate using at least one global alignment mark from the first and second sets of global

[ ] This application claims the benefit under 35 U.S.C. §119(e) of U.S. Provisional Application(s) No(s).:

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Country	Appln. No.	Filed

from which priority under Title 35 United States Code, § 119 is claimed

[ ] is enclosed.

[ ] will follow.

[X] Address all future correspondence to:

Paul J. Farrell, Esq.
DILWORTH & BARRESE LLP
333 Earle Ovington Boulevard
Uniondale, New York 11553
(516) 228-8484

Date: **January 25, 2001**

SIGNATURE OF ATTORNEY

Paul J. Farrell

Reg. No. **33,494**

DILWORTH & BARRESE LLP
333 Earle Ovington Blvd.
Uniondale, NY 11553
Tel. No. (516) 228-8484
Fax (516) 228-8516

alignment marks as a reference point.

13. A circuitry package having first and second circuit systems, each of said systems having means for wirelessly communicating with each other through at least one substrate.

14. The circuitry package according to Claim 13, wherein the first and second circuit systems have identical operational formats.

15. The circuitry package according to Claim 13, wherein the first and second circuit systems have different operational formats.

16. The circuitry package according to Claim 13, wherein the at least one substrate is transparent.

17. The circuitry package according to Claim 13, wherein the first and second circuit systems are one of a communication device and a chip.

18. The circuitry package according to Claim 13, wherein the first and second circuit systems are fabricated on the at least one substrate.

19. The circuitry package according to Claim 13, wherein the first and second circuit systems are bonded to the at least one substrate.

20. The circuitry package according to Claim 13, wherein the circuitry package is fabricated by an alignment process which includes the steps of:

providing a photoresist on a top and bottom side of said at least one substrate;

irradiating said photoresist from at least one side of said at least one substrate to form an alignment pattern on said top and bottom side of said at least one substrate;

etching said alignment pattern to form global alignment marks on said top and bottom sides of said at least one substrate; and

providing at least one communication device on one side of said at least one substrate using at least one global alignment mark as a reference point.

21. The circuitry package according to Claim 13, wherein the first and second circuit systems include first and second interconnection structures for interconnecting the components of the first and second circuit systems, respectively.

22. The circuitry package according to Claim 21, wherein the first and second interconnection structures are connected to a substrate.

23. The circuitry package according to Claim 13, wherein the at least one substrate includes alignment marks for aligning the at least one substrate with alignment marks of another substrate.

24. The circuitry package according to Claim 13, wherein the circuitry package is fabricated by an alignment process which includes the steps of:

providing an opaque layer on one side of said at least one substrate;

providing a photoresist on said opaque layer on one side of said at least one substrate;

irradiating said photoresist from at least the one side of said at least one substrate to form a first alignment pattern on said one side of said at least one substrate;

etching said first alignment pattern to form a first set of global alignment marks on said one side of said at least one substrate;

providing a photoresist on the other side of said at least one substrate;

irradiating said first alignment pattern from at least the one side of said at least one substrate to form a second alignment pattern on the other side of said at least one substrate;

etching said second alignment pattern to form a second set of global alignment marks on the other side of said at least one substrate, wherein the first and second sets of global alignment marks align with respect to each other; and

providing at least one communication device on said one side of said at least one substrate using at least one global alignment mark from the first and second sets of global alignment marks as a reference point.

25. A method for fabricating a circuitry package comprising the steps of:

providing a photoresist on a top and bottom side of a substrate;

irradiating said photoresist from the at least one side of the substrate to form an alignment pattern on said top and bottom side of said substrate;

etching said alignment pattern to form global alignment marks on said top and bottom sides of said substrate; and

providing at least one circuit system on one side of said substrate using at least one global alignment mark as a reference point.

26. The method according to Claim 25, further comprising the step of providing at least one circuit system on the other side of said substrate using at least another global alignment mark as a reference point, wherein said at least one global alignment mark and said at least another global alignment mark are respectively aligned.

27. The method according to Claim 26, further comprising the steps of:

providing a first interconnection structure to interconnect the components of the at least one circuit system on the one side of said substrate; and

providing a second interconnection structure to interconnect the components of the at least one circuit system on the other side of said substrate.

28. The method according to Claim 27, further comprising the step of connecting the first and second interconnection structures to a substrate.

29. The method according to Claim 25, further comprising the step of aligning global alignment marks of at least one substrate to the global alignment marks of the substrate.

30. A method for fabricating a circuitry package comprising the steps of:

providing an opaque layer on one side of a substrate;

providing a photoresist on said opaque layer on one side of said substrate;

irradiating said photoresist from at least the one side of said substrate to form a first

alignment pattern on said one side of said substrate;

etching said first alignment pattern to form a first set of global alignment marks on said one side of said substrate;

providing a photoresist on the other side of said substrate;

irradiating said first alignment pattern from at least the one side of said substrate to form a second alignment pattern on the other side of said substrate;

etching said second alignment pattern to form a second set of global alignment marks on the other side of said substrate, wherein the first and second sets of global alignment marks align with respect to each other; and

providing at least one communication device on said one side of said substrate using at least one global alignment mark from the first and second sets of global alignment marks as a reference point.

31. The method according to Claim 30, further comprising the step of providing at least one communication device on the other side of said substrate using at least another global alignment mark from the first and second sets of global alignment marks as a reference point, wherein said at least one global alignment mark and said at least another global alignment mark are respectively aligned.

32. The method according to Claim 30, wherein the substrate is transparent.